Image

BUR920030096US1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:
Steven H. Voldman

Group Art Unit: Unknown

Serial No.: ~~Not assigned yet~~ 10/707,069

Examiner: unknown

Filed: ~~Concurrently herewith~~ 11/19/2003

For: METHODOLOGY FOR PLACEMENT BASED ON CIRCUIT FUNCTION AND LATCHUP SENSITIVITY

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT UNDER 37 C.F.R. 1.56

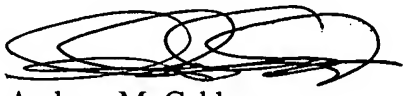
Sir:

Under provisions of 37 C.F.R. 1.97 through 1.99 and pursuant to applicant's duty of disclosure under 37 C.F.R. 1.56, applicants respectfully bring the documents listed on the attached Form PTO-1449 to the attention of the Examiner in charge of the above-identified application. A copy of the documents cited is enclosed for the convenience of the Examiner.

This citation does not constitute an admission that the cited references are relevant or material to the claims nor should it be construed as a representation that no other art than that identified exists. They are merely cited as constituting related art of which the applicant is aware.

It is respectfully requested that this documents be considered by the Examiner and formally made of record in this application.

Respectfully submitted,



Andrew M. Calderon
Reg. No. 38,093

McGuireWoods LLP
1750 Tysons Boulevard, Suite 1800
McLean, VA 22102
(703)712-5000

SUPPLEMENTAL FORM PTO-1449 (Modified) LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)	ATTY. DOCKET NO. BUR920030096US1	SERIAL NO. Unassigned
	APPLICANT: Steven H. Voldman	
	FILING DATE: Concurrently Herewith	GROUP: Unassigned

REFERENCE DESIGNATION

U.S. PATENT DOCUMENTS

EXAMINER INITIALS		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (IF APPRO.)

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
							YES	NO

OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)

			T. Aoki, "A Practical High-Latchup Immunity Design Methodology for Internal Circuits in the Standard Cell-Based CMOS/BiCMOS LSI's", IEEE Transactions on Electron Devices, Vol. 40, No. 8, August 1993.
			B. Basaran, et al., "Latchup-Aware Placement and Parasitic-Bounded Routing of Custom Analog Cells", IEEE, 1993.
			H. de La Rochette, et al., "The Effect of Layout Modification on Latchup Triggering in CMOS by Experimental and Simulation Approaches"; IEEE Transactions on Nuclear Science, Vol. 41, No. 6, December 1994.
			S. Bhattacharya, et al., "Design Issues for Achieving Latchup-free, Deep Trench-Isolated, Bulk, Non-Epitaxial, Submicron CMOS", IEDM, 1990.
			M. Ker, et al., "New Experimental Methodology to Extract Compact Layout Rules for Latchup Prevention in Bulk CMOS IC's", IEEE Custom Integrated Circuits Conference, 1999.
			M. Ker, et al., "Layout Design and Verification for Cell Library to Improve ESD/Latchup Reliability in Deep-Submicron CMOS Technology", IEEE Custom Integrated Circuits Conference 1998.

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.